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09/887,021	06/25/2001	Terry R. Lee	M4065.0407/P407	6645

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,021	LEE, TERRY R.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20,22-33 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20,22-33 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20, 22-33 and 35 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 5-9, 11-12, 14-16, 18-20, 24, 26-27, 29-31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Applicant's Admitted Prior Art (hereinafter AAPA).

As to claim 1, Robertson teaches a circuit card (memory module 100) comprising: a circuit element supported by the circuit card, the circuit element having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B); a plurality of signal lines supported by the circuit card, each signal line being electrically connected respectively to one of said plurality of inputs or one of said plurality of outputs (Fig. 1A and col. 3, lines 47-67); and a plurality of shields (106) (at least col. 3 lines 60-62); wherein said signal lines are grouped in a plurality of adjacent corresponding pairs, a shield being located respectively on each side of each of said plurality of corresponding pairs of said signal lines (Fig. 2B and col. 4, lines 57-67). Robertson teaches shields located on each side of the signal pair (at ground pins), however, Robertson does not explicitly disclose shields that extend the

entire length of the signal to the circuit card and supported by the circuit card. AAPA teaches shields that extend the entire length of the signal to the circuit card and supported by the circuit card (Fig. 3 and paragraph [0008-0009]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement shields that extend the entire length of the signal to the circuit card and supported by the circuit card as taught by AAPA in the system of Robertson to reduce cross-talk along the entire signal lines.

As to claim 2, Robertson further teaches each said shield line is a ground shield (ground) (col. 3, lines 62-67).

As to claim 5, Robertson further teaches the circuit element is a memory device (col. 4, lines 5-21).

As to claims 6, 8, 11, 15, 18, Robertson teaches a circuit card comprising: a plurality of signal lines (103) supported by the circuit card, each signal line being arranged and configured to be electrically connected at a first end respectively to one of a plurality of connectors of a connector device mounted on a printed circuit board (Fig. 1A and col. 3, lines 47-67); a circuit element (e.g. 107 or the interface of 107 where input/output signals go in/out) mounted to the circuit card and having a plurality of inputs and a plurality of outputs (Figs. 1A, 1B), said signal lines being electrically connected at a second end respectively to one of said plurality of inputs or outputs (Fig. 1A and col. 3, lines 47-67); and a plurality of shields (106), the shields being arranged and configured to be electrically connected at a first end to respective connectors of said connector device mounted on said printed circuit board, (Fig. 2B and col. 4, lines 57-67); said signal lines

being grouped in a plurality of adjacent corresponding pairs, respective ones of said shields being located on each side of each of said plurality of corresponding pairs of said signal lines; wherein said signal lines are part of a bus system (ground shields are arranged between a pair of signal lines) (Fig. 2B and col. 4, lines 57-67). Robertson teaches shields located on each side of the signal pair (at ground pins), however, Robertson does not explicitly disclose shields that extend adjacent and the length of the signal to the circuit card and supported by the circuit card. AAPA teaches shields that extend the entire length of the signal to the circuit card and supported by the circuit card (Fig. 3 and paragraph [0008-0009]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement shields that extend the entire length of the signal to the circuit card and supported by the circuit card as taught by AAPA in the system of Robertson to reduce cross-talk along the entire signal lines.

As to claims 7, 9, 12, Robertson further teaches said shields are ground shields (ground) (col. 3, lines 62-67).

As to claim 14, Robertson further teaches the connector is adapted for connection to a motherboard (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 16, Robertson further teaches each said shield is a ground shield (ground) (col. 3, lines 62-67).

As to claims 19, 26, 30, 33, Robertson teaches a processing system comprising: a processing unit (e.g. CPU 1001); a connector device (102) having a plurality of pins and electrically connected to said processing unit and a circuit card (memory module 100) coupled to said processing unit through said connector device (col. 5 lines 40-59 and

Figs. 4, 5), said circuit card comprising: a circuit element supported by the circuit card and having a plurality of inputs and outputs (Figs. 1A, 1B); a plurality of signal lines (103) supported by the circuit card, each of said plurality of signal lines being coupled respectively between one of said plurality of inputs and one of plurality of pins, or one of said plurality of outputs and one of plurality of pins (ground shields are arranged between a pair of signal lines) (Fig. 2B and col. 4, lines 57-67); a plurality of shields, each shield being connected respectively to said circuit element, said signal lines being grouped in a plurality of adjacent corresponding pairs, a shield being located between respective corresponding pairs of said signal lines (two signal pins 104 are arranged between a pair of ground pins) (Figs. 1A, 1B, 2B and col. 4, lines 57-67, wherein said processing system comprises a bus system for passing signals through said processing system and said signal lines are coupled to said bus system (Figs. 4-5 and col. 5 line 40 to col. 6 line 3As to claim 20, Robertson further teaches the shield is a ground shield (ground) (col. 3, lines 62-67). Robertson teaches shields located on each side of the signal pair (at ground pins), however, Robertson does not explicitly disclose shields that extend the entire length of the signal to the circuit card and supported by the circuit card. AAPA teaches shields that extend the entire length of the signal to the circuit card and supported by the circuit card (Fig. 3 and paragraph [0008-0009]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement shields that extend the entire length of the signal to the circuit card and supported by the circuit card as taught by AAPA in the system of Robertson to reduce cross-talk along the entire signal lines.

As to claim 20, Robertson further teaches each said shield is a ground shield (ground) (col. 3, lines 62-67).

As to claim 24, Robertson further teaches said circuit element is a memory device (col. 4, lines 5-21).

As to claim 27, Robertson further teaches shields are a ground shields (ground) (col. 3, lines 62-67).

As to claim 29, Robertson further teaches a motherboard, equipped with a connector adapted for connection of said memory expansion card to said motherboard, the connector comprising connecting pins corresponding respectively to said signal lines and said shields (col. 3, lines 47-66 and col. 4, lines 40-59).

As to claim 31, Robertson further teaches said shields are a ground shields (ground) (col. 3, lines 62-67).

3. Claims 3 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Applicant's Admitted Prior Art (hereinafter AAPA) and further in view of Chin et al. (6,216,205) (hereinafter Chin).

As to claim 3, the argument above for claim 1 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said circuit element. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

As to claim 22, the argument above for claim 19 applies. However, Robertson does not explicitly disclose a driver to drive the signals between said inputs and said outputs of said circuit element. Chin teaches driver (I/O driver 16) to drive signals between inputs and outputs of an integrated circuit memory device (col. 8, lines 28-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a driver as taught by Chin in the integrated circuit memory device of Robertson to for transferring data to and from the memory device (col. 8, lines 32-39).

4. Claims 4, 10, 13, 17, 23, 28, 32, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Applicant's Admitted Prior Art (hereinafter AAPA), and further in view of Ortega et al. (6,527,587) (herein after Ortega).

As to claim 4, the argument above for claim 1 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 10, the argument above for claim 8 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential

signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 13, the argument above for claim 11 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 17, the argument above for claim 15 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 23, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 28, the argument above for claim 26 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 32, the argument above for claim 30 applies. However, Robertson does not explicitly disclose the signals in each of said corresponding pairs are differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

As to claim 35, the argument above for claim 33 applies. However, Robertson does not explicitly disclose adapting said first plurality of connectors in each corresponding pair to conduct differential signals. Ortega teaches differential signals (col. 1, lines 49-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement differential signals as taught by Ortega in the system of Robertson to suppress signal noise and/or cross-talk (col. 1, lines 49-52).

5. Claims 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Robertson et al. (6,658,530) (hereinafter Robertson) in view of Applicant's Admitted Prior Art (hereinafter AAPA), and further in view of Elabd (6,526,462).

As to claim 25, the argument above for claim 19 applies. However, Robertson does not explicitly disclose the processing unit and the circuit element are on a same chip. Elabd teaches implementing the processor, memory, control unit, etc... on the same chip (col. 1, lines 22-54). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processor and the integrated circuit on the same chip as taught by Elabd in the system of Robertson to provide a product that is smaller and faster (col. 1, lines 26-31).

Response to Arguments

6. Applicant's arguments filed 04-10-06 have been fully considered but they are not persuasive:

With respect to Applicant's argument that Robertson teaches ground pins and one "would ***not be motivated*** to follow the teaching of the AAPA to add shields that extend the entire length of the signal to the circuit cards, but would instead be motivated by Robertson to eliminate the shields of AAPA and simply provide ground connector pins" (pages 12-16 of the Remarks): it is noted that the novel aspect in the claimed invention is shields located on each side of every pair of signal lines to minimize the number of pins required on the connector (as admitted in the specification). Specifically, AAPA discloses conventional systems implement shields (60) on each side of every signal line (B0, B1, B2) (Fig. 3) to reduce signal cross-talk on the bus, however, it almost double the number of pins required on the connector. Therefore an improved system is desired in which the shields are located on each side of every pair of signal lines to minimize the number of pins required on the connector. Robertson teaches shields located on

each side of every pair of signal lines to minimize the number of pins required on the connector (Fig. 1). However, Robertson does not disclose shielding the entire length of the signals, not just shielding at the pins. Since AAPA discloses shielding the entire length of a signal lines is being used in conventional system, one of ordinary skill in the art would recognize the benefit of having ***the entire length of signal lines shielded to reduce cross-talk along the entire signal lines***, compared to ***just reduce cross-talk at the pins***. Thus, the Examiner disagreed Applicant's argument that there is no motivation to combine, and the rejection set forth above is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha Vu whose telephone number is 571-272-3643. The examiner can normally be reached on Mon-Thur and alternate Fri 8:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Trisha Vu
Examiner
Art Unit 2112

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REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
6/23/06